REMARKS

Claims 1-22 are pending in the application. Claims 16-19 are withdrawn from consideration.

Approval of the attached drawing changes in order to avoid the objections raised in the Office Action is requested. New drawing Figures 26 and 27 have been inserted in the application to illustrate the subject matter of claims 13-15.

Page 4 and 5 of the specification have been amended to avoid the concerns noted in items 2 and 3 in the Office Action.

Withdrawal of the rejection of claims 13-15 under 35 U.S.C. § 112, is requested. Claim 21 has been amended to show two transistors, rather than one. The subject matter of amended claim 21 includes only that subject matter originally disclosed in the specification, particularly in original claims 13-15, which form part of the disclosure.

Withdrawal of the objection to claims 13-15 under 35 U.S.C. § 112, is requested. The specification discloses the use of n-epi, which stands for the conventional n-dioped epitaxial layer in a semiconductor product. Further, claim 13 has been amended to make clear that the single crystal extrinsic base is made from SiGe.

Withdrawal of the rejection of claims 1-3, 5, 7, 9, 11 and 12 under 35 U.S.C. § 102(b) as being anticipated by Khajezadeh (U.S. Pat. No. 4,202,006), is requested. The present invention as exemplified by claim 1 provides for a semiconductor wafer with improved ESD robustness. In carrying out the invention of independent claim 1, first and second semiconductor devices are provided on a wafer. The first semiconductor device, which as disclosed in the specification may be a bipolar transistor, is designed with a subcollector which is a doped region adjacent the collector of the device. The second semiconductor device may be either a bipolar transistor or a diode of the type disclosed in the specification. The second semiconductor device has increased ESD robustness due to the specific doping material or concentration of material in the subcollector, as compared to the first device. Thus, employing the invention of claim 1 permits a

semiconductor wafer to have ESD protection on devices which have external connections where ESD protection is needed, while having interior components such as the first semiconductor device with a subcollector which is doped differently to provided improved device performance, such as a high frequency transistor. Thus, implementing the invention provides for ESD protection where it is needed most.

Referring specifically to amended claim 1, the second semiconductor device includes a subcollector which is doped, to provide lateral ballasting of the second subcollector. The lateral ballasting of the second subcollector provides the ESD protection necessary for devices connected to external end connections of the semiconductor wafer.

Turning now to the Khajezadeh (U.S. Pat. No. 4,202,006) reference, a device is disclosed which has multiple semiconductor devices. The reference fails to disclose or suggest any provisions for providing an increased ESD robustness to any device on the substrate. The disclosed device is used to increase the breakdown voltage of a semiconductor device, but the problem of increasing breakdown voltage is not the same as providing for ESD robustness. ESD robustness is a measure of a devices ability to dissipate a current introduced through an electrostatic discharge. Breakdown voltage is a measure of a devices ability to withstand conducting of a current across a reverse biased junction.

The cited reference fails to disclose doping the second subcolletor in a manner which will increase the ESD robustness of that device over the ESD robustness of the first semiconductor device per claims 1, 19 and 21. Instead, a doping condition is selected to increase breakdown voltage which is an unrelated problem.

It is submitted that the foregoing claimed structure is not disclosed or suggested in the cited reference. While the disclosed changes in doping levels may have other uses, the claimed control over ESD protection is not disclosed or suggested in the prior art reference. The fact that ESD protection can result by providing lateral ballasting of the second subcollector, per claim 1, remains totally undisclosed in the cited reference.

Withdrawal of the rejection of claims 1-5, 7-9, 11 and 12 under 35 U.S.C. § 102(b) as being anticipated by Ohkawa et al. (U.S. Pat. No. 5,798,560), is requested. It is not seen where Ohkawa et al. discloses or suggests the two subcollectors, wherein one has a doping level for providing ballasting for improved ESD robustness. While substrates with multiple devices having multiple subcollectors are known from these references, a configuration which provides one device with an increased ESD robustness over the other is undisclosed.

Withdrawal of the rejection of claims 1-3, 5, 7, 11 and 12 as being anticipated under 35 U.S.C. § 102(b) by Yamaguchi (63-288055 JPO), is requested. From the English abstract of the reference, there is no disclosure of any structure which would provide the foregoing benefits of increased ESD robustness for one semiconductor device. While the circuit may include devices with both arsenic and antimony as buried layers, there is no suggestion that they will be selected so that ballasting of the second subcollector increases ESD robustness for one of the devices.

Withdrawal of the rejection of claims 4 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Khajezadeh (U.S. Pat. No. 4,202,006), is requested. In reviewing the reference, it does not disclose any indication of the implant dosage range of rejected claims 4 and 6. The allegation that it would have been obvious to select such ranges is not supported by the record, but is a general conclusion of the discredited "obvious to try standard." Further, the allegation that the reference discloses the claimed sheet resistance for the subcollector, since it would have been obvious to one skilled in the art that better emitter efficiency higher inverse beta at relatively low breakdown voltages would occur from an optimum value, still fails to disclose the effects on ESD robustness as presently claimed. Since the reference fails to show the structure, or the beneficial result of increased ESD robustness, it is not seen how it can yield or suggest the subject matter of the claims.

Application No.: 09/991,142 Docket No.: 21806-00134-US

Withdrawal of the rejection of claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Khajezadeh (U.S. Pat. No. 4,202,006), further in view of Herbert et al. (U.S. Pat. No. 6,365,447), is requested. Claim 10 depends on claim 1 and carries all the limitations thereof. Accordingly, claim 10 is also considered to be allowable.

Withdrawal of the rejection of claims 13-15 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi (63-288055), further in view of Kamins et al. (U.S. Pat. No. 5,633,179) and further in view of Chantre et al. (U.S. Pat. NO. 6,436,782), is requested. The rationale stated in the Office Action in support of the rejection is based on the observation that it would have been obvious to include the SiGe layer and p-doped based region in Yamaguchi in view of Kamins et al. (U.S. Pat. No. 5,633,179) in order to form an intrinsic and extrinsic base that reduces base resistance and hence increases operation speed. This observation is not derived from any considerations regarding ESD robustness, where the second transistor has a subcollector, different from the first transistor subcollector.

Accordingly, the combination of the mosaic of references proposed, is not the result of any suggestions contained in the references, or the prior art in general, and therefore do not form the necessary evidentiary bases in which to reject the application.

In view of the foregoing, favorable reconsideration of the application is requested and an early allowance is solicited.

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Respectfully submitted,

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